38. (Amended) The method, as in Claim 36, further comprising [the step of]:

generating an internal column address subsequent to the first external column address for operation in the burst mode, the internal column address patterned after the first external column address.

39. (Amended) The method, as in Claim 36, further comprising [the step of]:

selecting at least one address pathway based on the selection between the burst mode and the pipelined mode.

Please add new claims as follows:

59. (New) A method of accessing a memory, comprising:

receiving an external row address;

choosing whether the memory is in a burst mode of operation or in a pipeline mode of operation;

selecting a read operation or a write operation for the memory; and

executing a read or write operation in the chosen mode of operation.

60. (New) The method of claim 59, and further comprising:

switching between a burst mode of operation and a pipelined mode of operation.

61. (New) The method of claim 59, and further comprising:

switching between a read operation and a write operation.

62. (New) The method of claim 59, wherein the operations are performed in a different order.

63. (New) A method of accessing a memory, comprising:

receiving an external row address;

selecting a burst mode of operation or a pipeline mode of operation of the memory;

selecting a read operation or a write operation for the memory;

selecting an external address only data path, obtaining an external column address, and obtaining information from the memory if the read operation of the pipeline mode of operation is selected;

selecting an external address only data path, obtaining an external column address, and providing information to the memory if the write operation of the pipeline mode of operation is selected;

selecting an initial buffered external address data path, obtaining an initial external column address, obtaining information from the memory, and generating internal column addresses and obtaining further information from the memory until all desired internal column addresses are used if the read operation of the burst mode of operation is selected; and

selecting an initial buffered external address data path, obtaining an initial external column address, providing information to the memory, and generating internal column addresses and proividing further information to the memory until all desired internal column addresses are used if the write operation of the burst mode of operation is selected.

64. (New) The method of claim 63, wherein the operations are performed in a different order.

65. (New) A method of operating a memory circuit, comprising:

receiving a mode select signal;

receiving an initial external address;

selecting a read or a write operation of the memory;

cycling a second enabling signal multiply between active and inactive;

generating an internal address on a cycle of the second enabling signal based on the initial external address;

changing the mode select signal to select a pipeline mode of operation while maintaining the first enabling signal in an active state; and

receiving an external address on each cycle of the second enabling signal.

66. (New) A method for accessing a memory, comprising:

maintaining a first enabling signal in an active state;

maintaining a mode select signal to select a burst mode of operation;
receiving an initial external address;
selecting a read or a write operation of the memory;
cycling a second enabling signal multiply between inactive and active;
generating an internal address on a cycle of the second enabling signal based on the initial external address; and
switching the mode of operation to a pipeline mode on successive cycles of the second enabling signal by changing the mode select signal.

67. (New) A method for operating a memory, comprising:
maintaining a first enabling signal in an active state;
maintaining a mode select signal to select a burst mode of operation;
selecting a read operation or a write operation of the memory;
receiving a stream of addresses and cycling a second enabling signal for processing the stream of addresses; and
changing the mode select signal to select a pipeline mode of operation.

68. (New) A method for data transfer direction selection in a memory, comprising:
selecting a read or a write operation of the memory;
selecting a burst or a pipeline mode of operation for the memory;
selecting an external address only data path, obtaining an external column address, and accessing the memory when the pipeline mode of operation is selected; and
selecting an initial buffered external address data path, obtaining an inital external column address, accessing the memory, and generating internal column addresses when the burst mode of operation is selected.

69. (New) A storage device comprising:
mode circuitry configured to select between a burst mode and a pipelined mode;
selection circuitry for selecting between a read operation and a write operation;
an external column address data path for pipeline read and write operation column